6. THE CLAIMS

It is claimed:

1. A method of determining at least one ratio of transistor sizes, the method comprising:

   a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a piece-wise-linear current source;

   b) determining a steady state solution to the sizing model; and

   c) determining at least one ratio of transistor sizes from the steady state solution.

2. The method of claim 1, further comprising:

   d) determining at least one dimension of a transistor based at least in part upon the ratio of transistor sizes.

3. The method of claim 1, wherein the act of creating a sizing model includes creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage.

4. The method of claim 1, wherein the act of creating a sizing model includes creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the

second current being greater than the first current, and the second voltage being greater than the first voltage.

5. The method of claim 1, wherein the act of creating a sizing model includes creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first current corresponding to the input capacitance of a first logic element, the second current corresponding to the input capacitance of a second logic element.

6. The method of claim 1, wherein the act of creating a sizing model includes creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first current being proportional to the input capacitance of a first logic element, the second current being proportional to the input capacitance of a second logic element.

7. The method of claim 1, wherein the act of creating a sizing model includes creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current

source is greater than the first voltage and less than or equal to a second voltage, the first current corresponding to the input capacitance of a first logic element, the second current corresponding to the input capacitance a second logic element, both the first logic element and the second logic element being of the same type and selected from the group of types: inverter, AND, NAND, OR, NOR, XOR, and multiplexer.

8. The method of claim 1, wherein the act of creating a sizing model includes creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first current being proportional to the input capacitance of a first logic element, the second current being proportional to the input capacitance of a second logic element, both the first logic element and the second logic element being of the same type and selected from the group of types: inverter, AND, NAND, OR, NOR, XOR, and multiplexer.

9. A device containing machine readable instructions, that when executed perform a method of determining at least one ratio of transistor sizes, the method comprising:

a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a piece-wise-linear current source;

b) determining a steady state solution to the sizing model; and

c) determining at least one ratio of transistor sizes from the steady state solution.

10. The device of claim 9, further containing computer readable instructions for:

d) determining at least one dimension of a transistor based at least in part upon the ratio of transistor sizes.

11. The device of claim 9, further containing computer readable instructions for creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage.

12. The device of claim 9, further containing computer readable instructions for creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the second current being greater than the first current, and the second voltage being greater than the first voltage.

13. The device of claim 9, further containing computer readable instructions for creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first

current corresponding to the input capacitance of a first logic element, the second current corresponding to the input capacitance of a second logic element.

14. The device of claim 9, further containing computer readable instructions for creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first current being proportional to the input capacitance of a first logic element, the second current being proportional to the input capacitance of a second logic element.

15. The device of claim 9, further containing computer readable instructions for creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first current corresponding to the input capacitance of a first logic element, the second current corresponding to the input capacitance of a second logic element, both the first logic element and the second logic element being of the same type and selected from the group of types: inverter, AND, NAND, OR, NOR, XOR, and multiplexer.

16. The device of claim 9, further containing computer readable instructions for creating a sizing model that includes a piece-wise-linear current source configured to (1) select a

first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the first current being proportional to the input capacitance of a first logic element, the second current being proportional to the input capacitance of a second logic element, both the first logic element and the second logic element being of the same type and selected from the group of types: inverter, AND, NAND, OR, NOR, XOR, and multiplexer.

17. An integrated circuit created at least in part by a method of determining at least one ratio of transistor sizes, the method comprising:

a) creating a sizing model by replacing at least one logic element in a circuit description with a sizing element that includes a piece-wise-linear current source;

b) determining a steady state solution to the sizing model; and

c) determining at least one ratio of transistor sizes from the steady state solution.

18. The integrated circuit of claim 17, wherein the integrated circuit was created at least in part by determining at least one dimension of a transistor based at least in part upon the ratio of transistor sizes.

19. The integrated circuit of claim 17, wherein the integrated circuit was created at least in part by creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage and (2) select a second current if the voltage at the

piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage.

20. The integrated circuit of claim 17, wherein the integrated circuit was created at least in part by creating a sizing model that includes a piece-wise-linear current source configured to (1) select a first current if the voltage at the piece-wise-linear current source is less than or equal to a first voltage, and (2) select a second current if the voltage at the piece-wise-linear current source is greater than the first voltage and less than or equal to a second voltage, the second current being greater than the first current, and the second voltage being greater than the first voltage.